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	Title	Pub. Date	Int. Class	App. N
1.	(WO 2007/008422) ELECTROCHEMICAL CELL HAVING A PARTIALLY **OXIDIZED** CONDUCTOR	18.01.2007	H01M 2/02	PCT/ US2006

An electrochemical cell having an aqueous electrolyte and an **electrode** with partially **oxidized** graphite mixed with an electroche graphite is **oxidized** on its surface and within a specified range of surface oxidation to improve the aqueous electrolyte's ability to The weight ratio of active material to graphite is maximized to improve performance on high drains tests.

2.	(WO 2005/040343) IMPROVED APPARATUS AND METHOD FOR IDENTIFICATION OF BIOMOLECULES, IN PARTICULAR NUCLEIC ACID SEQUENCES, PROTEINS, AND ANTIGENS AND ANTIBODIES	06.05.2005	G01N 15/06	PCT/ US2004

An electrical detection system and method using an array of conductive sense sites within a sensing substrate for electrically dete hybridization or binding reaction between two chemical substances, particularly between biogenic substances such as nucleotide antigens and antibodies. The method and apparatus provide a an inexpensive, robust, small, repeatable, and intuitively easy to u or low levels of hybridization with large numbers of closely spaced conductive sense sites within a single substrate.

3.	(WO 2005/024487) PROGRAMMABLE OPTICAL COMPONENT FOR SPATIALLY CONTROLLING THE INTENSITY OF BEAM OF RADIATION	17.03.2005	G02B 26/08	PCT/ IB2004/

A programmable optical component (10) for spatially controlling the intensity of a beam of radiation (b), which component compri which is divided in programmable elements (4,6,8), characterized in that each programmable element comprises bendable nano- switchable between a **non**-bend state (S) and a bend state (S') by means of a driver field. In their bend state the nano-elements a programmable element may be a switchable diffraction grating or a programmable mask.

4.	(WO 2005/010891) FERROELECTRIC AND HIGH DIELECTRIC CONSTANT INTEGRATED CIRCUIT CAPACITORS WITH THREE-DIMENSIONAL ORIENTATION FOR HIGH DENSITY MEMORIES, AND METHOD OF MAKING THE SAME	03.02.2005	G11C 11/22	PCT/ US2004

activities regarding patents and

the PCT

A three-dimensional ('3-D') memory capacitor comprises a bottom **electrode**, a ferroelectric thin film, and a top **electrode** that co insulator layer. The capacitance area is greater than the horizontal footprint area of the capacitor. Preferably, the footprint of the nm2, and the corresponding capacitance area is typically in a range of from 0.4 nm2 to 1.0 nm2 The ferroelectric thin film prefera exceeding 60 nm. A capacitor laminate including the bottom **electrode**, ferroelectric thin film, and the top **electrode** preferably ha 200 nm. A low-thermal-budget MOCVD method for depositing a ferroelectric thin film having a thickness in a range of fr...

5. (WO 2004/095607) **ELECTROD**ES COMPRISING MIXED ACTIVE PARTICLES — 04.11.2004 — H01B 1/06 — PCT/US2004

Electrode active materials comprising two or more groups of particles having differing chemical compositions, wherein each grou material selected from: (a) materials of the formula A1aM1b(XY4)cZd; and (b) materials of the formula A2eM2fOg; and wherein (or K; (ii) M1 and M3 comprise a transition metal; (iv) XY4 a phosphate or similar moiety; and (v) Z is OH, or halogen. In a preferre A3hMniO4 having an inner and an outer region, wherein the inner region comprises a cubic spinel manganese oxide, and the ou manganese oxide enriched in Mn+4 relative to the inner region. In a preferred embodiment, the compositions also comprise a ba

6. (WO 2004/066307) STACKED MEMORY CELL HAVING DIFFUSION BARRIERS — 05.08.2004 — H01L 21/02 — PCT/US2004

A bottom **electrode** (238) and portion of an insulator layer (224) adjacent to the bottom **electrode** of a memory capacitor (540) a form sidewall (440) and a moat region (450) in the insulator. A nonconductive oxygen barrier layer (460) is deposited to cover the moat. The nonconductive oxygen barrier layer and a conductive diffusion barrier (444, 236) beneath the capacitor together provid diffusion barrier between the capacitor and a switch (208). A nonconductive hydrogen barrier layer (508), the nonconductive oxyg conductive diffusion barrier substantially completely envelop the capacitor, in particular a ferroelectric thin film (490) in the capac...

7. (WO 2004/049441) LOW THERMAL BUDGET FABRICATION OF FERROELECTRIC MEMORY USING RTP — 10.06.2004 — C30B 29/32 — PCT/US2003

A layered superlattice material precursor is applied to a substrate (102). The precursor coating is rapid thermal processed (RTP) C/second at a hold temperature in a range of from 500 °C to 900 °C for a cumulative heating time not exceeding 30 minutes, and minutes. In fabricating a ferroelectric memory cell (100), the coating is heated in oxygen using RTP, then a top **electrode** layer (substrate including the coating is heated using RTP in oxygen or in nonreactive gas after forming the top **electrode** layer. The th thickness in a range of from 25 nm to 120 nm. The process typically has a thermal budget value not exceeding 95...

8. (WO 2003/099715) SYNTHESIS OF METAL COMPOUNDS USEFUL AS CATHODE ACTIVE MATERIALS — 04.12.2003 — C01B 13/14 — PCT/US2003

Active materials of the invention contain at least one alkali metal and at least one other metal capable of being **oxidized** to a high other metals are accordingly selected from the group consisting of transition metals (defined as Groups 4-11 of the periodic table **non**-transition materials such as tin, bismuth, and lead. The active materials may be synthesized in single step reactions or in mu one of the steps of the synthesis reaction, reducing carbon is used a s a starting material. In one aspect, the reducing carbon is p carbon, preferably in particulate form such as graphites, amorphous carbon, carbon blacks and the like. In another ...

9. (WO 2003/085771) ALKALI-IRON-COBALT PHOSPHATES AND RELATED **ELECTRODE** ACTIVE MATERIALS — 16.10.2003 — C01B 25/45 — PCT/US2003

Electrode active materials, preferably having an olivine structure, of the formula: AaMbXY4 wherein (a) A is one or more alkali m a ≤ 2; (b) M is one or more metals, comprising Co and Fe, 0 < b ≤ 2; and (c) XY4 is X'O 4-x'Y'x,X'04-y'Y'2y, X'S4, or a mixture the Si, Ge, V, S, or a mixture thereof; X' is P, As, Sb, Si, Ge, V, or a mixture thereof; Y' is halogen, S, N, or a mixture thereof; 0 ≤ x < 0.8 ≤ a ≤ 1.2, and 0.9 ≤ b ≤ 1. In a preferred embodiment, M further comprises one or more **non**-transition elements. Also provide batteries comprising an **electrode** active material of this invention.

10. (WO 2003/049172) LANTHANIDE SERIES LAYERED SUPERLATTICE MATERIALS FOR INTEGRATED CIRCUIT APPLICATIONS — 12.06.2003 — H01L 21/02 — PCT/US2002

An integrated circuit (40) includes a layered superlattice material (57) including one or more of the elements cerium, praseodymiu promethium, samarium, europium, gadolinium, terbium, dysprosium, holmium, erbium, thulium, ytterbium, and lutetium. These el elements or superlattice generator elements in the layered superlattice material. In one embodiment, one or more of these eleme a bismuth layered material. They also are preferably used in combination with one or more of the following elements: strontium, c cadmium, lead, titanium, tantalum, hafnium, tungsten, niobium, zirconium, bismuth, scandium, yttrium, lanthanum, antimony, chr

11. (WO 2003/023380) ASSAY BUFFER, COMPOSITIONS CONTAINING THE SAME, AND METHODS OF USING THE SAME — 20.03.2003 — C12Q 1/48 — PCT/US2002

Compositions, reagents, kits, systems, system components, and methods for performing assays. More particularly, the invention combinations of reagents to provide improved assay performance.

12. (WO 2003/023365) ELECTROCHEMICAL SENSOR USING INTERCALATIVE, REDOX-ACTIVE MOIETIES — 20.03.2003 — C12N 15/09 — PCT/US2002

Compositions and methods for electrochemical detection and localization of genetic point mutations, common DNA lesions and c perturbations within oligonucleotide duplexes adsorbed onto **electrode**s and their use in biosensing technologies are described. active moiety (such as an intercalator or nucleic acid-binding protein) is adhered and/or crosslinked to immobilized DNA duplexes from an **electrod**e and probed electrochemically in the presence or absence of a **non**-intercalative, redox-active moiety. Interrup electron-transfer caused by base-stacking perturbations, such as mutations or binding of a protein to its recognition site are refle

13. (WO 2003/017353) PROVIDING PHOTONIC CONTROL OVER WAFER BORNE SEMICONDUCTOR DEVICES — 27.02.2003 — G01R 31/27 — PCT/US2002

Disclosed are methods for providing wafer photonic flow control to a semiconductor wafer (1700) having a substrate (1720), at le and at least one surface layer (1710). Photonic flow control can be achieved through the formation of trenches (1725) and/or insu formed in said wafer (1700), whereby active regions (1760) are defined by trenches (1725) that operate as nonconductive areas systems for wafer level burn-in (WLBI) of semiconductor devices are also disclosed. Photonic flow control at the wafer level is im methods and systems.

14. (WO 2003/017352) PROVIDING CURRENT CONTROL OVER WAFER BORNE SEMICONDUCTOR DEVICES USING OVERLAYER PATTERNS — 27.02.2003 — G01R 31/27 — PCT/US2002

Disclosed are methods for providing wafer parasitic current control to a semiconductor wafer (1240) having a substrate (1240), a (1240) and at least one surface layer (1240). Current control can be achieved through the formation of patterns (1240) surroundi patterns (1240) including insulating implants and/or sacrificial layers formed between active devices represented by said contacts through active regions (1260) associated with said contacts (1215) and active devices. Methods of and systems for wafer level b semiconductor devices are also disclosed. Current control at the wafer level is important when using WLBI methods and systems

15. (WO 2003/017325) PROVIDING CURRENT CONTROL OVER WAFER BORNE SEMICONDUCTOR DEVICES USING TRENCHES — 27.02.2003 — G01R 31/27 — PCT/US2002

Disclosed are methods for providing wafer parasitic current control to a semiconductor wafer (1500) having a substrate (1520), a (1565) and a surface layer (1510), and electrical contacts (1515) formed on said surface layer (1510). Current control can be ach trenches (1525) around electrical contacts, where electrical contacts and associated layers define an electronic device. Insulating placed into trenches (1525) and/or sacrificial layers (1540) can be formed between electronic contacts (1515). Trenches control c

16. (WO 2003/003498) HYDROGEN STORAGE BATTERY; POSITIVE NICKEL **ELECTRODE**; POSITIVE **ELECTROD**E ACTIVE MATERIAL AND METHODS FOR MAKING — 09.01.2003 — H01M 4/26 — PCT/US2002

A hydrogen storage battery with improved cycle life and a method for making the same. The battery has a negative **electrode** wi active negative material and a negative **electrode** capacity and a positive **electrode** electrochemically coupled with the negative **electrode** having a positive **electrode** capacity and an electrochemically active positive material with a precharge. Also describe **electrode** material for a hydrogen storage battery and a method for making the same. The positive **electrode** material includes a material which is partially **non-oxidized**. The preoxidized material may be used to provide a precharge to the positive **electrode**.

17. (WO 2002/091473) FERROELECTRIC COMPOSITE MATERIAL, METHOD OF MAKING SAME AND MEMORY UTILIZING SAME — 14.11.2002 — H01L 21/02 — PCT/US2002

A ferroelectric memory (436) includes a plurality of memory cells (73, 82, 100) each containing a ferroelectric thin film (15) includi composite material having a ferroelectric component (18) and a dielectric component (19), the dielectric component being a differ than the ferroelectric component. The dielectric component is preferably a fluxor, i.e., a material having a higher crystallization ve component. The addition of the fluxor permits a ferroelectric thin film to be crystallized at a temperature of between 400 °C and 5

18. (WO 2002/073680) METHOD OF MAKING LAYERED SUPERLATTICE MATERIAL WITH ULTRA-THIN TOP LAYER — 19.09.2002 — H01L 21/02 — PCT/US2002

In the manufacture of an integrated circuit memory cell, a strontium bismuth tantalate or strontium bismuth tantalum niobate thin on a substrate (26, 49) and a carefully controlled UV baking process is performed on the strontium bismuth tantalate layer (50) p ultra-thin bismuth tantalate layer (51). A second **electrode** (52) is formed on top of the ultra-thin bismuth tantalate layer (51).

19. (WO 2002/073669) METHOD OF MAKING LAYERED SUPERLATTICE MATERIAL WITH IMPROVED MICROSTRUCTURE — 19.09.2002 — H01L 21/02 — PCT/US2001

In the manufacture of an integrated circuit, a first **electrode** (48) is formed on a substrate (28). In a first embodiment, a strontium and a second **electrode** (52) are formed on top of the first **electrode** (48). Prior to the final crystallization anneal, the first **electro** bismuth tantalate layer (50) and the second **electrode** (52) are patterned. The final crystallization anneal is then performed on th embodiment, a second layer (132) of strontium bismuth tantalate is deposited on top of the strontium bismuth tantalate layer (50) second **electrode** (52) on top of the first and second layers (50), (132). In a third embodiment, a carefully con...

20. (WO 2002/065536) RAPID-TEMPERATURE PULSING ANNEAL METHOD AT LOW TEMPERATURE FOR FABRICATING LAYERED SUPERLATTICE MATERIALS AND MAKING ELECTRONIC DEVICES INCLUDING SAME — 22.08.2002 — C23C 18/12 — PCT/US2001

A liquid precursor for forming a layered superlattice material (124, 226, 610) is applied (324) to an integrated circuit substrate. Th annealed in oxygen using a rapid-temperature pulsing anneal ('RPA') technique with a ramp rate of 30 °C/second at a hold tempe time of 30 minutes. The RPA technique includes applying a plurality (330, 340) of rapid-temperature heat pulses in sequence.

21. (WO 2002/004887) METHODS AND APPARATUS FOR PROCESSING MICROELECTRONIC WORKPIECES USING METROLOGY — 17.01.2002 — H01L 21/00 — PCT/US2001

A method and apparatus for processing a microelectronic workpiece using metrology. The apparatus can include one or more pr metrology unit (228), and a control unit (270) coupled to the metrology unit and at least one of the processing or transport unites. a process recipe or a process sequence of the processing unit based on a feed forward or a feed back signal from the metrology can include, a seed layer disposition unit, a process layer electrochemical disposition unit, a seed layer enhancement layer(232), polishing unit, and/or an annealing chamber arranged for sequential processing of a workpiece. The processing units can be con

22. (WO 2001/076771) LOW TEMPERATURE OXIDIZING METHOD OF MAKING A LAYERED SUPERLATTICE MATERIAL — 18.10.2001 — C30B 7/00 — PCT/US2001

A thin film of precursor for forming a layered superlattice material (124, 226, 624) is applied (324, 424) to an integrated circuit sub then a strong oxidizing agent is applied (328, 330, 426, 428) at low temperature in a range of from 100° C to 300° C to the precur forming a metal oxide thin film. The strong oxidizing agent may be liquid or gaseous. An example of a liquid strong oxidizing ager example of a gaseous strong oxidizing agent is ozone. The metal oxide thin film is crystallized by annealing (336, 338, 432, 434) range of from 500° C to 700° C, preferably not exceeding 650° C, for a time period in a range of from 30 minutes...

23. (WO 2001/067516) RAPID RAMPING ANNEAL METHOD FOR FABRICATING SUPERLATTICE MATERIALS — 13.09.2001 — C30B 7/00 — PCT/US2001

A liquid precursor for forming a layered superlattice material is applied (324) to an integrated circuit substrate (122, 224, 508). Th annealed in oxygen using a rapid ramping anneal ("RRA") technique (328) with a ramping rate of 50 °C/second at a hold tempera time of 30 minutes.

24. (WO 2001/066834) CHEMICAL VAPOR DEPOSITION PROCESS FOR FABRICATING LAYERED SUPERLATTICE MATERIALS — 13.09.2001 — C23C 16/02 — PCT/US2001

A first reactant gas is flowed (310) into a CVD reaction chamber (430) containing a heated integrated circuit substrate. The first r precursor compound or a plurality of first precursor compounds, and the first precursor compound or compounds decompose in t deposit a coating containing metal atoms on the heated integrated circuit substrate. The coating is treated (312) by RTP. Thereat flowed (316) into a CVD reaction chamber (430) containing the heated substrate. The second reactant gas contains a second pre plurality of second precursor compounds, which decompose in the CVD reaction chamber to deposit more metal atoms on the su

25. (WO 2001/024237) INTEGRATED CIRCUITS WITH BARRIER LAYERS AND METHODS OF FABRICATING SAME — 05.04.2001 — H01L 21/02 — PCT/US2000

A hydrogen diffusion barrier (132, 124, 332, 324, 432, 424, 532, 524, 720, 710, 750, 770, 912) in an integrated circuit (100, 200, 900) is located to inhibit diffusion of hydrogen towards a dielectric thin film (128, 328, 428, 528, 711, 764, 906) of metal oxide ma diffusion barrier comprises at least one of the following oxides: tantalum pentoxide; tungsten oxide; aluminum oxide; titanium oxi ferroelectric or high-dielectric, nonferroelectric material. Preferably, the metal oxide comprises ferroelectric layered superlattice m diffusion barrier layer may be a single continuous layer (132) completely overlying a common plate **electrode** and the diele...

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